Remarks

Applicants respectfully request reconsideration of this application as amended. No claims have been amended. No claims have been cancelled. Therefore, claims 1-20 are presented for examination.

Claims 1-11, 13-15, and 19-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over MacDonald (U.S. Patent No. 6,295,574) in view of Simpson (EP0742522A), and further in view of Maupin (U.S. Patent No. 6,154,832). Applicant submits that the present claims are patentable over MacDonald in view of Simpson and further in view of Maupin.

In order to establish a *prima facie* case of obviousness there must first be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, *the prior art reference (or references when combined) must teach or suggest all the claim limitations*." (Emphasis added). *In re Vaech*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). Manual of Patent Examining Procedure (MPEP), 8th Edition, Revision 2, May 2004, §2143. Applicant submits that there is no motivation to combine MacDonald, Simpson and Maupin.

MacDonald discloses a CPU that includes a real time interrupt control unit configured to control real time capabilities of the CPU. See MacDonald at Abstract. MacDonald further discloses that instead of using interrupt acknowledge cycles normally used to locate an interrupt vector, an interrupt descriptor is stored in a real time interrupt register which is coupled to the real time interrupt control unit. This causes the real time interrupt control unit

to rapidly determine the fetch address of the real time interrupt. See MacDonald at col. 3, ll. 50-63.

Simpson discloses arbiter circuitry connected to storage circuitry for determining the priority status of each interrupt signal and selecting the one interrupt signal with the highest priority status. The arbiter circuitry then outputs an interrupt identifier associated with the selected interrupt signal. See Simpson at col. 1, ll. 46-56.

Maupin discloses a processor employing multiple register sets to eliminate interrupts. Maupin further discloses that one register is dedicated to interrupt sources, and another is dedicated to (non-interrupt) tasks. See Maupin at Abstract. Maupin discloses providing service routines for the processor for requests typically made by signaling interrupts. See Maupin at col. 2, ll. 24-26. The service routines are stored in the register dedicated to interrupt sources. The service routines are then executed by accessing the register. See Maupin at col. 2 ll. 65 – col. 3 ll. 4. Accordingly, the use of these service routines eliminates interrupt signals from the processor. See Maupin at col. 4, ll. 17-18.

Claim 1 of the present application recites generating a real-time interrupt indicating a request to process real time data at a central processing unit (CPU), and determining whether the real-time interrupt has a higher priority than a non-real time operation being processed at the CPU. Applicant submits that there is no motivation to combine MacDonald, Simpson and Maupin. As discussed above, the system in MacDonald is directed at handling real time interrupts in CPUs, Simpson relates to arbiter circuitry that is used to determine the priority level of various interrupts, and Maupin is a processor employing multiple sets of registers to eliminate interrupts. Applicant submits that it would not be obvious to combine the cited references since Maupin is eliminating interrupts, as opposed to generating them, while

MacDonald and Simpson rely on the generation of interrupts. Because Maupin teaches away from MacDonald and Simpson, claim 1 is patentable over MacDonald in view of Simpson and further in view of Maupin.

Claims 2-6 and 17-18 depend on claim 1 and contain additional features, thus claims 2-6 and 17-18 are also patentable over MacDonald in view of Simpson and further in view of Maupin.

Claim 7 recites a central processing unit (CPU) to generate a real-time interrupt upon receiving real-time analog data and to process data associated with the real-time interrupt if the real-time interrupt has a higher priority than a non-real-time operation currently being processed. Thus, for the reasons described above with respect to claim 1, claim 7 is also patentable over MacDonald in view of Simpson and further in view of Maupin. Since claims 8-12 and 19-20 depend on claim 7 and contain additional features, claims 8-12 and 19-20 are also patentable over MacDonald in view of Simpson and further in view of Maupin.

Claim 13 recites an event mechanism to generate real-time interrupts in response to receiving real-time data stored within a register, and an event handler to process data associated with the real-time interrupts received upon determining that relative priority between the real-time interrupts and non-real-time operations being processed. Thus, for the reasons described above with respect to claim 1, claim 13 is also patentable over MacDonald in view of Simpson and further in view of Maupin. Since claims 14-16 depend on claim 13 and contain additional features, claims 14-16 are also patentable over MacDonald in view of Simpson and further in view of Maupin.

Claims 12 and 16-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over MacDonald in view of Simpson, further in view of Williams et al. (U.S. Patent No.

5,764,582). Applicants submit that the present claims are patentable over any combination of MacDonald, Simpson, Maupin and Williams.

Williams discloses a bus that communicates data between a digital signal processor and a hardware interface, which includes digital-to-analog and analog-to-digital converters. See Williams at col. 4, ll. 26-28. However, Williams does not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU. Additionally, MacDonald and Simpson do not disclose or suggest such a feature. The Examiner acknowledges in an Office Action that the reference of MacDonald in view of Simpson does not clearly indicate that higher priority is assigned to real-time interrupts. See Office Action mailed June 30, 2005 at page 3, paragraph 3. Since MacDonald, Simpson or Williams do not disclose or suggest determining whether a real-time interrupt has a higher priority than a non-real time operation being processed at a CPU, any combination of MacDonald, Simpson and Williams would not disclose or suggest the feature. Therefore, the present claims are patentable over MacDonald in view of Simpson, further in view of Williams.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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